



Interleaved Coupled DC/DC Converter Design for an Aircraft Supercapacitor-Based Energy Storage System

Abdullahi Abubakar^{1*}, Sulaiman Haruna Sulaiman¹, Ismaila Mahmud¹, Ibrahim Abdulwahab¹,
Hamza Mustapha¹, Muhammad Madaki^{1,2}

¹Department of Electrical Engineering, Ahmadu Bello University, Zaria-Nigeria.

²Defence Industries Cooperation of Nigeria (DICON), Kaduna, Nigeria

*Corresponding author: bakarabduull@gmail.com; ORCID: 0000-0003-0911-0153

DOI: <https://doi.org/10.xxxx/xxxx>

ABSTRACT

Keywords:

coupled inductor,
DC/DC converter,
DC bus,
Energy storage system,
Supercapacitor

Article History:

Received: 15/08/2026

Revised: 01/10/2026

Accepted: 09/10/2026

Published: 18/10/2026

Article Info:

Homepage: <https://zjeet.com.ng>

Volume: 15, No. 1, 2026

Pages: 102-118

This paper investigates the integration of a Supercapacitor (SC) energy storage system with a four-channel interleaved bidirectional DC/DC converter employing coupled inductors for aircraft applications. Due to the high peak power demand during the aircraft take-off phase, a high-power energy storage system is required to meet this requirement. The SC energy storage system, owing to its high-power density despite its low energy capacity, is considered suitable for high-power pulsed load applications. Various SC packs designs are investigated to achieve an optimal energy storage weight. A four-channel interleaved bidirectional DC/DC converter with coupled inductors is interfaced with the SC pack. The interleaved configuration is intended to provide equal current sharing among the channels while potentially reducing current ripple and current stress within the converter. Simulation results are presented to demonstrate the charging and discharging operation of the bidirectional DC/DC converter over a wide range of SC pack voltages. Experimental results are also provided to validate the simulation findings.

1. INTRODUCTION

The concept of the More Electric Aircraft (MEA) involves replacing conventional pneumatic, hydraulic, and mechanical systems with electrically driven power systems. This transition is motivated by the need to improve system efficiency, achieve higher power density, reduce emissions, and lower maintenance requirements. In MEA architectures, electrical energy is utilised to supply critical subsystems, including the Engine Generator Set (EGS), landing gear, and wing anti-icing systems. While MEA partially electrifies conventional subsystems thereby reducing fuel consumption, the All-Electric Aircraft (AEA)

represents a more radical approach, in which conventional systems are fully replaced by electrical systems with the objective of achieving net-zero emissions [1], [2].

The AEA relies on electrochemical energy sources such as batteries, supercapacitors, and fuel cells to support both propulsion and onboard power demands. However, significant challenges arise due to the high peak power requirements during take-off, where substantial power is needed to meet load demands. In addition, transient power fluctuations within the aircraft electrical system can introduce disturbances and affect overall system stability [3]. Existing

literature has explored the design of single energy storage systems, such as battery- or fuel cell-based solutions, to meet the energy requirements of AEA missions and onboard power generation. More recent studies [4–6] have investigated hybrid energy storage systems combining batteries and supercapacitors, where the battery provides the primary energy supply and the supercapacitor delivers peak power during transient conditions. This hybrid approach mitigates battery stress and contributes to improvements in the overall weight and performance of the energy storage system.

This work focuses on the design of a supercapacitor-based energy storage system to meet the peak power demand of an aircraft during the take-off phase. The proposed system comprises designing an optimised storage configuration integrated with a bidirectional power converter interfaced to a 270 V aircraft DC bus. The incorporation of the ESS necessitates a DC/DC converter to facilitate bidirectional power flow between the storage system and the DC bus. To minimise the overall system weight, a review of various converter topologies is conducted. Among the available options, bidirectional half-bridge converters which combine boost and buck operating modes are particularly well suited for ESS applications due to their simple structure and efficient switch utilization [7], [8]. In such configurations, the low-voltage side is connected to the ESS, while the high-voltage side interfaces with the DC bus.

Given the wide range of converter topologies, bidirectional DC/DC converters commonly employed in ESS applications are generally classified into isolated and non-isolated categories [9–11]. These converters are widely adopted due to their versatility in interfacing with different ESS technologies. Compared to their isolated counterparts, non-isolated DC/DC converters are often preferred because of their simpler structure, lower cost, and reduced weight and volume [9], [12–14]. However, conventional non-isolated converters are typically limited to low-power applications, as increasing the power level leads to higher stress on power switches and reduced converter efficiency. In addition, the selection of appropriate filter capacitance, inductance, and switching frequency

presents a significant design challenge. Although higher switching frequencies enable a reduction in passive component size thereby improving system dynamic response but also introduces increased switching losses.

To address these limitations, higher-power converters can be realised by employing a non-coupled interleaving technique. This approach improves passive component utilisation at higher switching frequencies, enhances power density, reduces current stress on individual power switches, and minimises losses in both active and passive components of the converter [15–18]. Although relatively straightforward to implement, this method requires larger magnetic components as the number of interleaved channels increases. While increasing the number of channels reduces the overall current ripple, the incremental benefit becomes negligible beyond a certain point [19–21]. Therefore, it is essential to determine the optimal number of channels for a given application. The sizing of the supercapacitor devices is based on commercially available cells. In addition, a four-channel interleaved power converter with coupled inductors is designed to interface the supercapacitor energy storage system with the aircraft DC bus. A phase-balancing strategy is implemented to ensure equal current sharing among the interleaved channels. This topology provides a reduced current ripple and is easier to control. However, with increasing number of interleaved channels, the current ripple reduction becomes less significant and with the increase in the size of magnetics which in turn increases the weight of the converter [22], [23]. The use of interleaved DC/DC converter with coupled inductors is proposed as it provides smaller ripple of voltage and current for the same size of magnetics. Furthermore, a mathematical model of the multiport interleaved converter is developed to enable both transient and steady-state analysis. The operation of the bidirectional converter is also presented to demonstrate performance across the full supercapacitor voltage range under both charging and discharging conditions. Finally, the simulation results are validated through experimental measurements.

2. OPTIMAL DESIGN OF SUPERCAPACITOR ENERGY STORAGE SYSTEM

This section investigates the optimal energy storage design required to meet the aircraft's peak power demand during the take-off phase. The peak power demand of the aircraft during take-off is 14 kW for a duration of 35 s [24], and a summary of this requirement is provided in Table 1.

Table 1: Supercapacitor power requirements.

Requirements	Values
Peak power	14 kW
DC bus Voltage	270 V
Take-off time	35 s

The supercapacitor (SC) must be integrated with a DC/DC power converter to enable bidirectional power flow, where the low-voltage side is interfaced with the SC and the high-voltage side is connected to the DC bus system. Ideally, the minimum voltage of the SC energy storage system (ESS) should be maintained at 50% of the DC bus voltage to ensure high efficiency and to reduce current stress on the converter passive components [3], [25]. This implies that discharging the SC from its maximum voltage down to 50% of its rated voltage allows approximately 75% of the stored energy to be utilised. This follows from the fact that the energy stored in a supercapacitor is proportional to the square of its voltage, i.e., $\frac{1}{2} CV^2$. Accordingly, for a depth of discharge (DoD) of 75%, the required energy can be expressed as:

For 75% DoD:

$$E_{req} = \frac{1}{2} C_{eqv} V_{max}^2 - \frac{1}{2} C_{eqv} V_{min}^2 \quad (1)$$

If the minimum voltage is defined as $V_{min} = 0.5 V_{max}$, then the extracted energy becomes:

$$E_{req} = \frac{1}{2} C_{eqv} (V_{max}^2 - 0.25 V_{min}^2)$$

$$E_{req} = \frac{1}{2} (0.75 \times C_{eqv} V_{min}^2) \quad (2)$$

where E_{req} is the required energy of the SC pack, C_{eqv} is the equivalent capacitance, and V_{max} and V_{min} represent the maximum and minimum voltages of the SC pack, respectively.

Significant long-term cycling experimentation conducted by [26] demonstrated only a 10%

degradation in the SC's end-of-life (EoL) performance after 30,000 cycles at 80% depth of discharge (DoD) and an operating temperature of 25 °C [27]. Therefore, as a design guideline to ensure long-term system performance, it is recommended to oversize the supercapacitor by approximately 30%–35% to account for 10%–30% EoL degradation [28]. An improved approach to supercapacitor sizing, as suggested by [29], aims to further reduce the required capacitance. Accordingly, the supercapacitor energy storage system is optimised based on the aircraft's peak power requirement. The equation used to determine the required energy, considering the aircraft DC bus voltage, is given in (3), while (4) provides the corresponding equivalent capacitance [24], [30]:

$$E_{req} = \frac{1}{2} \times \frac{C_{eqv}(V_{max}^2 - V_{min}^2)}{3600} \quad (3)$$

$$E_{req} = \frac{1}{2} C_{eqv} (V_{max}^2 - 0.25 V_{min}^2) = \frac{1}{2} (0.75 \times C_{eqv} V_{min}^2) \quad (4)$$

where E_{req} is the required energy of the SC pack, C_{eqv} is the equivalent capacitance, V_{max} and V_{min} represent the minimum and maximum voltage of the SC pack voltage respectively. The terms V_{cell} and C_{scap} are the SC cell voltage and capacitance respectively.

To interface with the DC/DC converter, the optimal selection of the SC maximum stack voltage is approximately 90% of the DC bus voltage [25]. This approach reduces the converter current ratings during the take-off discharge phase; as the supercapacitor stack discharges, its voltage decreases, requiring the converter to meet the peak power demand through duty-cycle adjustment. Furthermore, the minimum SC voltage is selected as 50% of its maximum value to limit the required peak current, which directly impacts the weight and volume of both passive and active components.

The cell capacitance and equivalent capacitance and are computed as 20.9 F and 1100 F, respectively, assuming a nominal cell voltage of 2.7 V (typical for most supercapacitor cells). This design necessitates higher stack voltages achieved through series connection, which increases the pack weight for a given energy level unless cells of different sizes with varying energy densities are considered. Since the interfaced

converter can accommodate lower stack voltages, a range of maximum supercapacitor unit voltages must be evaluated to determine the optimum stack weight. Ref. [24] considers commercially available supercapacitor cells within the range of 50 F to 5000 F, taking into account their specific energy characteristics. The optimisation process is carried out over the supercapacitor stack voltage range, from 90% of V_{max} down to 50% of V_{min} . Figure 1 presents the optimised supercapacitor pack weight and corresponding cell capacitances at different stack voltages, with the ULTIMO cell exhibiting the minimum weight. A summary of the design parameters is provided Table 2

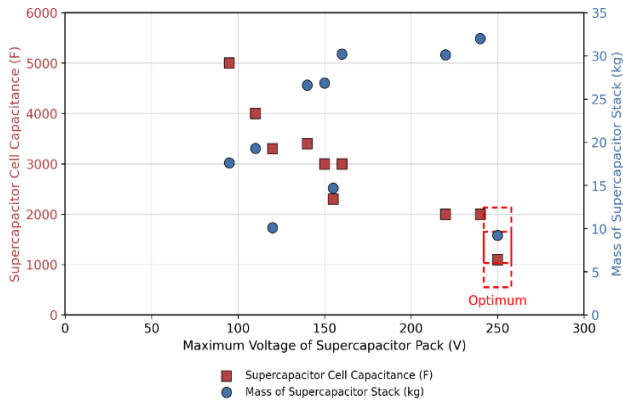


Fig. 1: SC stack weights at with their respective cell capacitances at varying maximum voltages.

Table 2: Design summary of the ULTIMO LIC cell [24].

Parameters	Value
Maximum voltage	250 V
Minimum voltage	125 V
Usable energy	136 Wh
Number of cells in series	66
Number of modules in parallel	1
Total cells	66
Cell capacitance	1100 F
Equivalent capacitance	20.9 F
Cell weight	0.14 kg
Total cell weight	9.21 kg

Based on the design SC ESS design, the DC/DC converter to be interfaced with is discussed in the next section.

2.1 Modelling of the four-channel interleaved

The four-channel interleaved converter consists of two coupled inductors of the same value are used to make a four-channel interleaved. The two coupled inductors

are phase shifted by 180° . The first coupled inductor having two channels is phase shifted by $0^\circ - 180^\circ$ and the other inductor is phase shifted by $90^\circ - 270^\circ$ to ensure an equal current ripple cancellation. The schematic circuit diagram of the bidirectional converter is shown in Figure 2. It consists of eight switches $S_1 - S_8$ with four legs and a combined digital control system feeding the converter through the PWM signal. Each of the leg has its complementary switch at 180° without deadtime consideration. The terms V_{bus} and v_{scap} are the DC bus and SC pack voltages. DC bus capacitance is denoted as C_{bus} with the current flowing through it as i_{DC} . The terms V_1, V_2, V_3 and V_4 are the voltages of the coupled inductors in each leg. The L_{s1}, L_{s2}, L_{s3} and L_{s4} are self inductances of the coupled inductors in the channels at i_1, i_2, i_3 and i_4 currents respectively. L_{m1} and L_{m2} are magnetizing inductances of each coupled inductor at leakage inductances of L_{k1} and L_{k2} . Common mode currents in the coupled inductors are denoted as i_{o1} and i_{o2} , the sum current to the SC ESS is represented as i_{scap} and C_{eqv} is the equivalent capacitance. The ESR in each channel are denoted as R_1, R_2, R_3 and R_4 while R_{k1} and R_{k2} represents the common mode inductances.

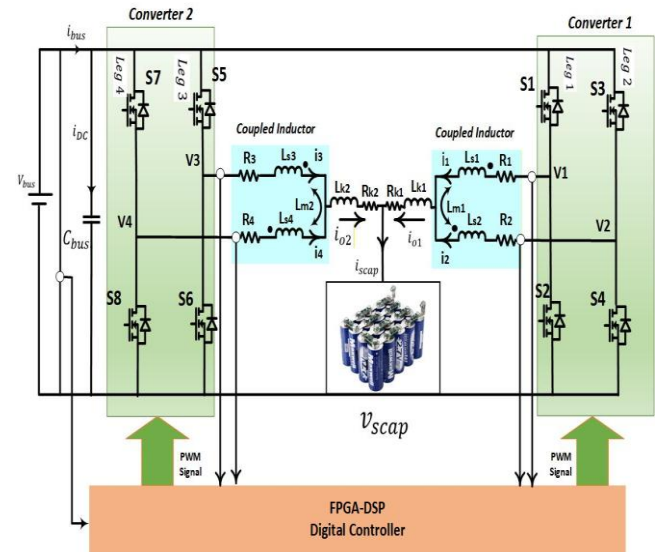


Fig. 2: Four channel interleaved converter system with coupled inductors showing also the convection of feedback signals to the digital control.

2.2 Principle of operation of the converter

There are four operating stages in one switching cycle of the converter and the circuit diagram for the different

switching stages with the direction of current flow are shown in the Figure 3 considering the charging mode condition. The operating conditions during discharging mode for different duty cycles, D at $D < 0.5$ and $D > 0.5$ are given. The different switching times of the converter from $t_0 - t_4$ are explained as follows:

Operating mode [$t_0 - t_1$]

- (a) The switches S_2, S_3, S_5 and S_7 are turned off. S_1, S_4, S_6 and S_8 are turned on in which the DC bus voltage energises the inductor L_{s1} linearly rising the current i_1 . The currents i_2, i_3 and i_4 in L_{s2}, L_{s3} and L_{s4} respectively decreases linearly. The current i_{o1} in the leakage inductance L_{k1} increases and i_{o2} in L_{k2} decreases linearly.
- (b) Four switches S_1, S_4, S_5 and S_7 are turned on in which the DC bus voltage energises the inductor L_{s1}, L_{s3} and L_{s4} thereby rising the currents i_1, i_3 and i_4 respectively. Only the current i_2 in L_{s2} decreases linearly to the output. The current i_{o1} in the leakage inductance L_{k1} decreases and i_{o2} in L_{k2} increases linearly.

Operating mode [$t_1 - t_2$]

- (a) Switches S_2, S_3, S_6 and S_8 are turned on while S_1, S_4, S_5 and S_7 are turned off. The DC bus voltage charges the inductor L_{s2} rising the current i_2 linearly. The currents i_1, i_3 and i_4 in the inductors L_{s1}, L_{s3} and L_{s4} respectively charges to the storage pack. On the output of the coupled inductors, the currents in the leakage inductors L_{k1} and L_{k2} increases and decreases the currents in i_{o1} and i_{o2} respectively.
- (b) Switches S_1, S_3, S_6 and S_7 are turned on while S_2, S_4, S_5 and S_8 are turned off. Currents i_1 in L_{s1}, i_2 in L_{s2} and i_4 in L_{s4} are energised through their switches by the input DC bus voltage while the current i_3 in inductor L_{s3} de-energises to the output

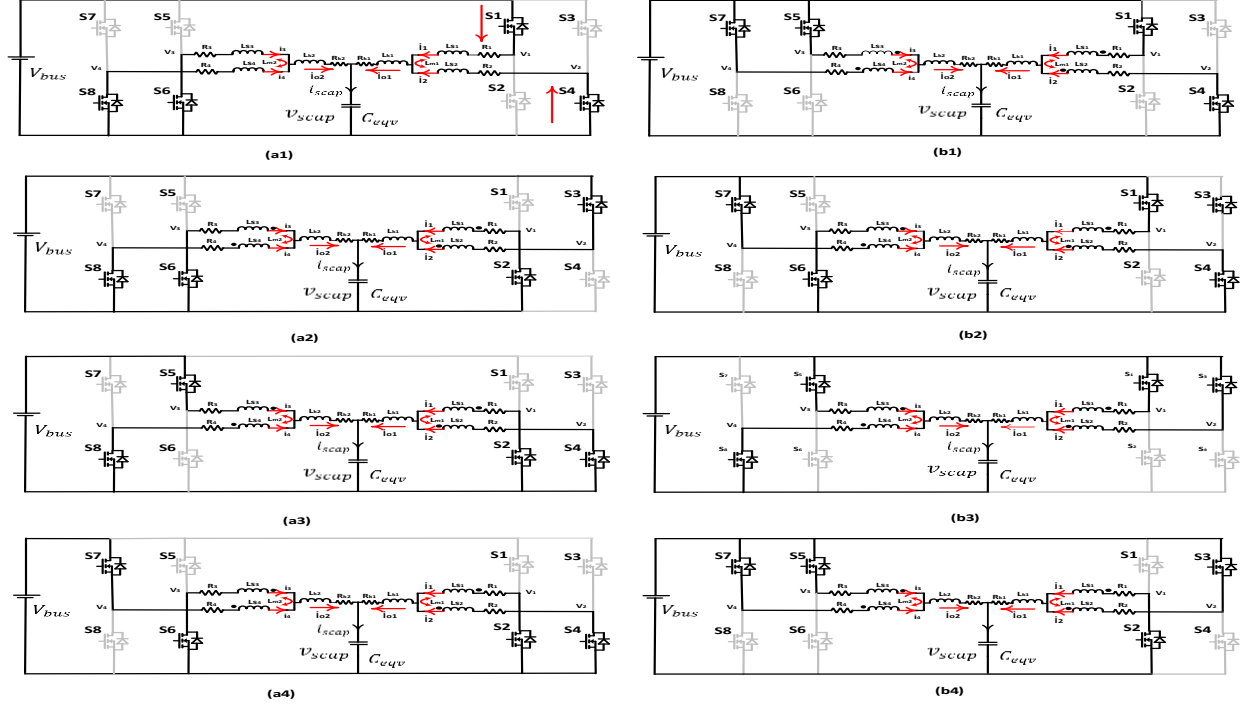
of the leakage inductor L_{k2} . The current i_{o1} in leakage inductor L_{k1} energises while i_{o2} in L_{k2} de-energises linearly.

Operating mode [$t_2 - t_3$]

- (a) Switches S_2, S_4, S_5 and S_8 are turned on, S_1, S_3, S_6 and S_7 are turned off. Currents in i_1, i_2 and i_4 are being charged to the SC voltage through their respective switches while the current i_3 in L_{s3} is charged linearly by the input DC bus voltage. The leakage current i_{o1} in L_{k1} is discharged while that of the i_{o2} is charged linearly.
- (b) Switches S_1, S_3, S_5 and S_8 are turned on while S_2, S_4, S_6 and S_7 are turned off. The DC bus voltage charges the current i_1, i_2 , and i_3 of inductor L_{s1}, L_{s2} and L_{s3} respectively, while the current i_4 in L_{s4} discharges linearly. The output leakage currents i_{o1} and i_{o2} charges and discharges linearly.

Operating mode [$t_3 - t_4$]

- (a) Switches S_2, S_4, S_6 and S_7 are turned on, S_1, S_3, S_5 and S_8 are turned off. The currents i_1, i_2 and i_3 in the inductors L_{s1}, L_{s2} and L_{s3} decreases linearly to the output of the leakage inductances while the DC bus voltage charges the inductor L_{s4} through S_7 , causing the rise of current linearly. At the output of the coupled inductances, the currents i_{o1} and i_{o2} of L_{k1} and L_{k2} respectively discharges and charges linearly.
- (b) Switches S_2, S_3, S_5 and S_7 are turned on, S_1, S_4, S_6 and S_8 are turned off. All the channel currents i_2, i_3 and i_4 are energised by the DC bus voltage causing the currents to flow linearly except the inductor L_{s1} . The current i_1 in the inductor L_{s1} is de-energised to the output. On the leakage side, the current i_{o1} in L_{k1} is de-energised while the current i_{o2} in L_{k2} is energised linearly.


 Fig. 3: Operating stages of the four-channel interleaved DC/DC converter at (a) $D < 0.5$ (b) $D > 0.5$

Assuming the ideal condition, the self-inductances and the ESR in the channels will be the same, that is:

$$\left. \begin{aligned} L_{S1} &= L_{S2} = L_S = L_{m1} + L_{k1} \\ L_{S3} &= L_{S4} = L_S = L_{m2} + L_{k2} \\ R_1 + R_{k1} &= R_2 + R_{k1} = R \\ R_3 + R_{k3} &= R_4 + R_{k2} = R \end{aligned} \right\} \quad (5)$$

The inductance relation can therefore be expressed as:

$$L_S = L_m + L_k \quad (6)$$

The relation of the magnetizing inductance in inversely coupled in the four channels is expressed as:

$$\left. \begin{aligned} V_1 + \alpha V_2 &= (1 - \alpha^2) L_S \frac{di_1}{dt} \\ V_2 + \alpha V_1 &= (1 - \alpha^2) L_S \frac{di_2}{dt} \\ V_3 + \alpha V_4 &= (1 - \alpha^2) L_S \frac{di_3}{dt} \\ V_4 + \alpha V_3 &= (1 - \alpha^2) L_S \frac{di_4}{dt} \end{aligned} \right\} \quad (7)$$

where V_1, V_2, V_3 and V_4 are the voltages applied to the corresponding windings of the coupled inductor, α is the coupling factor.

The dynamic equations for each operating stages of the converter are therefore analysed as:

$$[(0)t_o, (D)t_1]$$

$$\left. \begin{aligned} V_1 &= V_{bus} - v_{scap} \\ V_2 &= -v_{scap} \\ V_3 &= -v_{scap} \\ V_4 &= -v_{scap} \\ C \frac{dv_{scap}}{dt} &= i_1 + i_2 + i_3 + i_4 \end{aligned} \right\} \quad (8)$$

Evaluating for $\frac{di_1}{dt}, \frac{di_2}{dt}, \frac{di_3}{dt}, \frac{di_4}{dt}$ from equations (7) and (8) and equating the term, $\frac{(1+\alpha)}{(1-\alpha^2)L_S}$ to be $\frac{1}{\Sigma L_S}$; this gives equations (9).

$$\left. \begin{aligned} \frac{di_1}{dt} &= \frac{V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}(1+\alpha)}{(1-\alpha^2)L_S} = \frac{V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}}{\Sigma L_S} \\ \frac{di_2}{dt} &= \frac{\alpha V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}(1+\alpha)}{(1-\alpha^2)L_S} = \frac{\alpha V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}}{\Sigma L_S} \\ \frac{di_3}{dt} &= \frac{\alpha V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}(1+\alpha)}{(1-\alpha^2)L_S} = \frac{\alpha V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}}{\Sigma L_S} \\ \frac{di_4}{dt} &= \frac{\alpha V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}(1+\alpha)}{(1-\alpha^2)L_S} = \frac{\alpha V_{bus}}{(1-\alpha^2)L_S} - \frac{v_{scap}}{\Sigma L_S} \\ \frac{dv_{scap}}{dt} &= \frac{i_1}{C_{eqv}} + \frac{i_2}{C_{eqv}} + \frac{i_3}{C_{eqv}} + \frac{i_4}{C_{eqv}} \end{aligned} \right\} \quad (9)$$

The matrix form for the dynamic equations is:

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_4}{dt} \\ \frac{dv_{scap}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ v_{scap} \end{bmatrix} + \begin{bmatrix} 1 \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ 0 \end{bmatrix} [V_{bus}] \quad (10)$$

From the state space equation, the matrix A_1 and B_1 are the state variables and input variables of the system respectively.

$$[(D)t_1, (0.5 - D)t_2]$$

Dynamic equation of the converter for the operation stage will be;

$$\left. \begin{aligned} V_1 &= -v_{scap} \\ V_2 &= V_{bus} - v_{scap} \\ V_3 &= -v_{scap} \\ V_4 &= -v_{scap} \\ C_{eqv} \frac{dv_{scap}}{dt} &= i_1 + i_2 + i_3 + i_4 \end{aligned} \right\} \quad (11)$$

After evaluating the inverse coupling equation, the matrix form is expressed as:

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_4}{dt} \\ \frac{dv_{scap}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ v_{scap} \end{bmatrix} + \begin{bmatrix} \alpha \\ (1-\alpha^2)L_s \\ 1 \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ 0 \end{bmatrix} [V_{bus}] \quad (12)$$

From the state space equation, the matrix A_2 and B_2 are the state variables and input variables of the system respectively.

$$[(0.5 - D)t_1, (D)t_2]$$

Dynamic equation of the converter for the operation stage will be

$$\left. \begin{aligned} V_1 &= -v_{scap} \\ V_2 &= -v_{scap} \\ V_3 &= V_{bus} - v_{scap} \\ V_4 &= -V_o \\ C_{eqv} \frac{dv_{scap}}{dt} &= i_1 + i_2 + i_3 + i_4 \end{aligned} \right\} \quad (13)$$

Evaluating the inverse coupling equation with the dynamic equation, the matrix form for the dynamic equations is:

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_4}{dt} \\ \frac{dv_{scap}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\sum L_s} \\ \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ v_{scap} \end{bmatrix} + \begin{bmatrix} \alpha \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ 1 \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ 0 \end{bmatrix} [V_{bus}] \quad (14)$$

From the state space equation, the matrix A_3 and B_3 are the state variables and input variables of the system respectively.

$$[(D)t_1, (0.5 - D)t_2]$$

At this operation stage, the equation for the converter dynamics is;

$$\left. \begin{aligned} V_1 &= -v_{scap} \\ V_2 &= -v_{scap} \\ V_3 &= -v_{scap} \\ V_4 &= V_{bus} - v_{scap} \\ C_{eqv} \frac{dv_{scap}}{dt} &= i_1 + i_2 + i_3 + i_4 \end{aligned} \right\} \quad (15)$$

This gives matrix form for the dynamic equations after equation with the inverse coupling equation.

$$\begin{aligned}
 \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_4}{dt} \\ \frac{dv_{scap}}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ v_{scap} \end{bmatrix} + \\
 &\begin{bmatrix} \alpha \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ \alpha \\ (1-\alpha^2)L_s \\ 1 \\ (1-\alpha^2)L_s \\ 0 \end{bmatrix} [V_{bus}] \quad (16)
 \end{aligned}$$

From the state space equation, the matrix A_4 and B_4 are the state variables and input variables of the system respectively.

Therefore, the state space averaging is obtained by averaging the state space equations of the four switching states as and the matrix is given in (17) and (18)

$$A = A_1(D) + A_2(0.5 - D) + A_3(D) + A_4(0.5 - D) \quad (17)$$

$$B = B_1(D) + B_2(0.5 - D) + B_3(D) + B_4(0.5 - D) \quad (18)$$

And the state space equations is expressed as

$$\begin{aligned}
 \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_4}{dt} \\ \frac{dv_{scap}}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ v_{scap} \end{bmatrix} + \\
 &\begin{bmatrix} \frac{1}{\Sigma L_s} \\ \frac{1}{\Sigma L_s} \\ \frac{1}{\Sigma L_s} \\ \frac{1}{\Sigma L_s} \\ \frac{1}{\Sigma L_s} \end{bmatrix} [V_{bus}]D \quad (19)
 \end{aligned}$$

The state space equation for small signal model is (20) such that the dynamic equation is transformed in (21)

where the coupled inductor voltages V_1, V_2, V_3 and V_4 are $\widetilde{d}_1 V_{dc}, \widetilde{d}_2 V_{dc}, \widetilde{d}_3 V_{dc}$ and $\widetilde{d}_4 V_{dc}$ respectively.

$$\tilde{x} = [A][x] + [B] \begin{bmatrix} \widetilde{d}_1 \\ \widetilde{d}_2 \\ \widetilde{d}_3 \\ \widetilde{d}_4 \end{bmatrix} [V_{bus}] \quad (20)$$

where $A = [i_1 \ i_2 \ i_3 \ i_4 \ v_{scap}]^T$ are the state matrixes of the system and $B = [\widetilde{d}_1 \ \widetilde{d}_2 \ \widetilde{d}_3 \ \widetilde{d}_4]^T$ are the input of the converter system.

The state space equation for the converter is given in equation (21) and taking the Laplace of the equation and converting to s-domain will determine the transfer function of the converter.

$$\begin{aligned}
 \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_4}{dt} \\ \frac{dv_{scap}}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ 0 & 0 & 0 & 0 & \frac{-1}{\Sigma L_s} \\ \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & \frac{1}{C_{eqv}} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ v_{scap} \end{bmatrix} + \\
 &\begin{bmatrix} \frac{1}{\Sigma L_s} & 0 & 0 & 0 \\ 0 & \frac{1}{\Sigma L_s} & 0 & 0 \\ 0 & 0 & \frac{1}{\Sigma L_s} & 0 \\ 0 & 0 & 0 & \frac{1}{\Sigma L_s} \end{bmatrix} \begin{bmatrix} \widetilde{d}_1 \\ \widetilde{d}_2 \\ \widetilde{d}_3 \\ \widetilde{d}_4 \end{bmatrix} [V_{bus}] \quad (21)
 \end{aligned}$$

2.3 Coupled Inductor Design

In designing the magnetics, the details of the coupled inductor for the two-channel interleaved is discussed. With the considered design constraint of 0.8A peak to peak ripple, the sum of the inductances, L_T is given by equation (22) and equation (23) gives the coupling factor, α as follows:

$$L_T = L_s + L_m = \frac{V_{bus} \times D}{2 \times \Delta I \times f_{sw}} \quad (22)$$

$$\alpha = \frac{L_m}{L_s} \quad (23)$$

where ΔI is the peak-to-peak ripple current, V_{bus} is the DC bus voltage, D the duty cycle at 50%, L_s and L_m are self and magnetizing inductances for the coupled inductor channel while f_{sw} is the switching frequency (20kHz).

The N27 UI ferrite core is used with core area is 840mm^2 . Other related core geometry are provided by the manufacturer's datasheet [31], [32]. The area product in selecting the coupled inductor magnetic core is given by the following relation:

$$A_c A_w = \frac{L_{eq} \times I_{pk}^2}{K_w \times B_m \times J} \quad (24)$$

where the A_c and A_w are core cross section area and winding area respectively, determined from the manufacturer's datasheet. I_{pk} is the peak current, B_m , J and K_w are the peak flux density, current density and the winding fill factor of the core respectively. L_{eq} is the equivalent inductance of the coupled inductor. The number of turns, N_T and the airgap, i_g are determined in equation (25) and (26) while equation (27) provides the expression for the magnetic field strength:

$$N_T = \frac{L_s \times I_{pk}}{B_m \times A_c} \quad (25)$$

$$i_g = \frac{\mu_o \times I_{pk} \times N_T}{B_m} \quad (26)$$

$$H = \frac{I_{DC} \times N_T}{l_m} \quad (27)$$

where N_T = number of turns on the primary or secondary (primary turns: secondary turns = 1:1), l_m is the magnetic path length, I_{DC} is the applied DC current, while $\mu_o = 4\pi 10^{-7} \text{H/m}$. The equivalent inductance, L_{eq} of the coupled inductance is given by the equation as:

$$L_{eq} = \frac{\mu_o \times \mu_{eff} \times A_c \times N_T^2}{l_m} \quad (28)$$

where μ_{eff} is the effective core permeability ($\mu_{eff} = \frac{l_m}{i_g}$). The calculated parameters values of the coupled inductor including the core geometry are summarised in Table 3.

Table 3: Coupled inductor core parameters.

Parameters	Symbol	Value
Peak flux density (T)	B_{max}	0.4
Total number of turns	N_T	120
Core area (mm^2)	A_c	840
Core window area (mm^2)	A_w	1695
Airgap (mm)	i_g	1.90
Magnetic path length (m)	l_m	0.258
Coupling factor	α	0.96
Magnetizing inductance (mH)	L_m	2.12
Self-inductance (mH)	L_s	2.16
Equivalent inductance (mH)	$L_{eq} \approx 4L_m$	8.12
Common mode inductance (mH)	L_k	1.50

2.4 Control Structure for the Interleaved DC/DC Converter

Referring to Fig 2 of the interleaved DC/DC converter, current control is implemented to regulate the channel currents in the interleaved channels. The control structure is presented as a block diagram in Figure 4. The PI controller is selected due to its simple control structure, as well as its ability to achieve fast dynamic response and high control accuracy. A PI current controller is implemented in each interleaved channel to maintain equal channel/winding currents and thereby prevent magnetic core saturation. From the control structure, the output load current reference on the SC side, $i_{scapref}$, is equally divided among the four interleaved channels (depending on the number of interleaved channels), resulting in equal reference currents i_{ref1} , i_{ref2} , i_{ref3} and i_{ref4} . These reference currents are then compared with the measured currents from the coupled inductor channels, i_1 , i_2 , i_3 , i_4 , as well as the calculated balancing currents, i_{ba1} and i_{ba2} . Each channel has its own PI controller to regulate the channel currents in the inter-cell transformers. The output of each PI controller provides the control signal, which is compared with a triangular carrier waveform to generate the PWM signals that serve as the gating signals for the half-bridge switches.

To achieve optimum switching ripple cancellation, the PWM signals are equally phase shifted by $360^\circ/N_{ch}$ between successive phases, where N_{ch} is the number of interleaved channels generated using a DSP-FPGA digital control platform. The phase-shift sequence is arranged such that the gate signal of each channel in the

coupled inductor is phase shifted by 180° with respect to its paired winding channel to achieve effective ripple cancellation. The assigned phase-shift angles for the first coupled-inductor channels are $i_1(0^\circ)$ and $i_2(180^\circ)$, while the other coupled-inductor channels are $i_3(90^\circ)$ and $i_4(270^\circ)$, operating at a switching frequency of 20 kHz. Consequently, the effective switching frequency at the common output point is 40 kHz for each coupled-inductor output. However, despite the applied phase shifting, current imbalance may still occur among the converter phases due to parasitic resistances and inductances in the converter components. This imbalance can result in increased thermal stress on the converter channels and switches, and may also lead to potential core saturation. Therefore, a phase-balancing strategy is implemented to mitigate these effects.

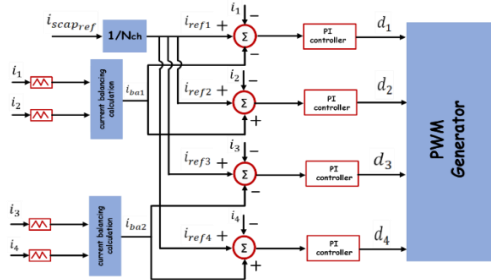


Fig. 4: Current control for the four interleaved channels with phase balance strategy

Implementing this strategy involves calculating the difference between the measured interleaved channel currents in each coupled inductor and dividing it by the number of interleaved channels. The calculated outputs, i_{ba1} and i_{ba2} , are then fed into their respective channels. These signals are subsequently summed with each reference current and the measured current of the interleaved system. The schematic in Figure 4 illustrates this process, and the equation governing the phase-balancing strategy is expressed as follows:

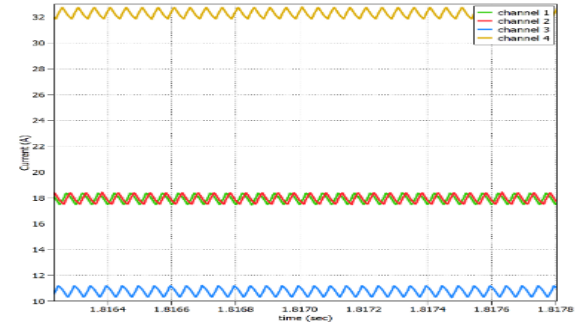
$$\begin{cases} i_{ba1} = \frac{i_1 - i_2}{2} \\ i_{ba2} = \frac{i_3 - i_4}{2} \end{cases} \quad (29)$$

3. SIMULATION RESULTS

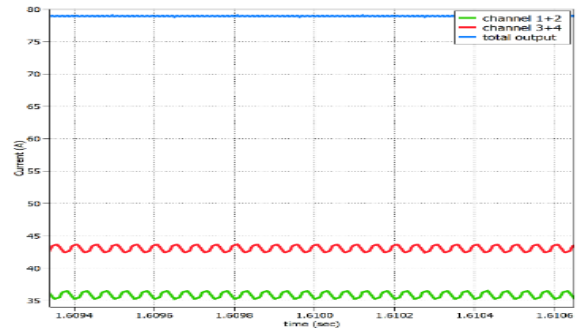
The DC/DC converter is simulated using the PLECS software. To analyse the current imbalance caused by variations in the parasitic elements, intentional variations are introduced into the parasitic components. The parasitic resistances considered in each channel,

R_1, R_2, R_3, R_4 , are assigned relatively small values to avoid significant power losses, namely $0.20 \, \Omega$, $0.20 \, \Omega$, $0.30 \, \Omega$, and $0.10 \, \Omega$, respectively. To visualise the effects of parasitic variations on the current imbalance, the simulation is initially operated in open loop mode at a duty cycle of 40% for all the channels. The resulting current waveforms are shown in Figure 5(a). Among the four channels, channel 4 exhibits the highest current of 32.3 A due to its lower parasitic resistance. In contrast, channel 3 carries the lowest current of 10.7 A as a result of its higher parasitic resistance, while channels 1 and 2 maintain balanced phase currents of 17.7 A each, collectively contributing to the total load current of 78.9 A.

The outputs of the two coupled inductors represent the common-mode currents, which correspond to the sum of the channel currents within each coupled inductor. The current imbalance in the two output channels (common-mode currents) is also influenced by the variations in the parasitic resistances of the interleaved channels, as shown in Fig 5(b). However, the total output current remains unchanged, as it is always equal to the sum of the phase currents in all channels.



(a)



(b)

Fig. 5: Current imbalance waveforms: (a) four channel interleaved (b) channel 1 and 2; sum of channel 3 and 4 and total output

3.1 Operation of the DC/DC converter under closed loop at transient and steady state

The simulation results for the transient response of the PI controller for the two channel converter were analysed at varying proportional gains, as illustrated in Figure 6(a)–(e), while maintaining a constant integral time until controller instability was observed. The channel currents (channels 1 and 2) were regulated at 3 A prior to the step change and at 4 A following the step change. The output current represents the sum of the channel currents, whereas the circulating current

represents the difference between the channel currents. It was observed that the controller exhibited the optimal response at a proportional gain of $k_p = 0.12$, achieving a fast settling time of 1.0 ms with a minimal current overshoot of 4%. However, as the proportional gain increased to $k_p = 0.92$, the current waveforms became oscillatory, thereby approaching instability. Since the control parameters remain consistent across all interleaved configurations, the same control parameters were applied to the control of the four-channel interleaved converter.

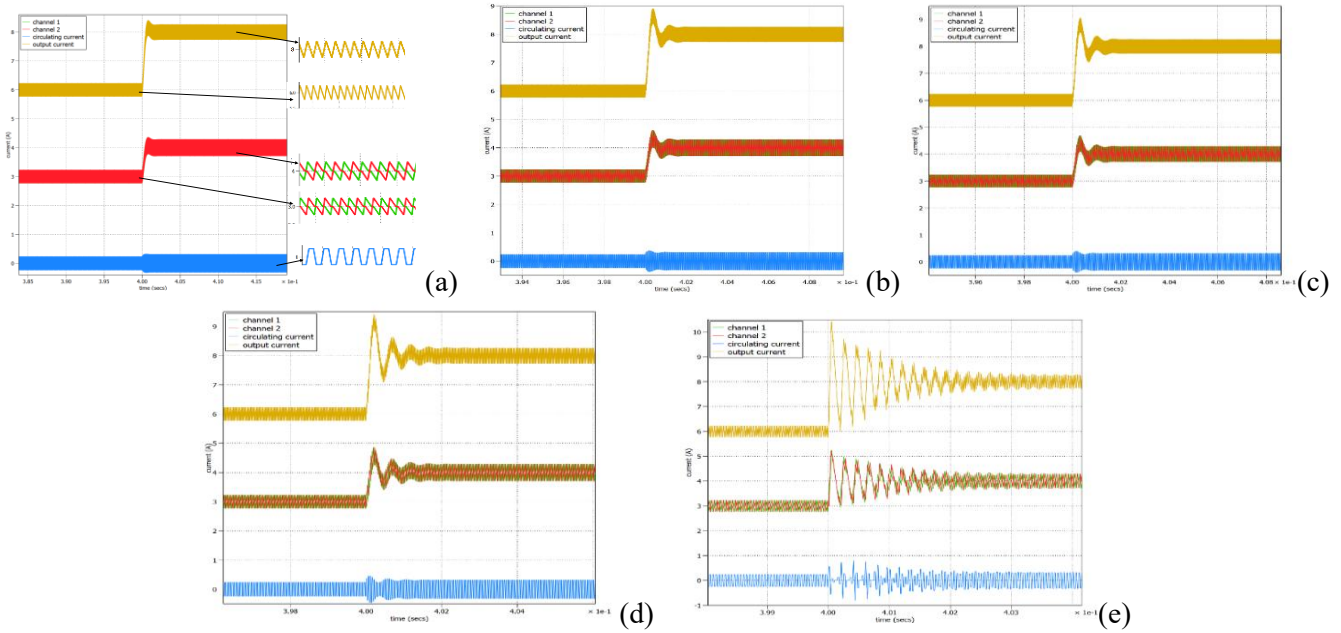


Fig. 6: Transient response at different PI controller gains (a) $k_p=0.12$ (b) $k_p=0.3$ (c) $k_p=0.4$ (d) $k_p=0.6$ (e) $k_p=0.92$

The DC/DC converter operating at 52% duty cycle in Figure 7 shows the simulation of the PWM gating signals of the converter switches phase with the coupled inductor 1 (e and f) and coupled inductor 2 (g and h) voltages in each of the windings.

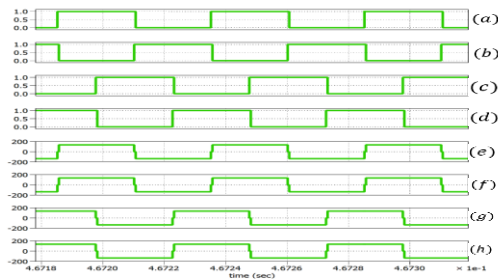


Fig. 7: High side switches PWM gating signals of Leg1, Leg2, Leg3 and Leg4 in (a) – (d); Line to line voltages coupled inductor 1 (Leg1 and Leg2) in (e) – (f); Line to line voltages coupled inductor 2 (Leg3 and Leg4) in (g) – (h)

Also, the interleaved channel currents, circulating current and the common mode current for one of the coupled inductors is also captured in Figure 8. It can be seen that the equal current in both channel 1 channel 2 and also in channel 3 and channel 4 both phases shifted by 180° results in eliminating their circulating current to zero, while their common mode currents result as the sum of the interleaved channel currents for each of the coupled inductor. On the left side of the Figure 8, shows the interleaved channel currents, circulating current as well as the sum of the channel currents at 52% duty cycle of coupled inductor 1 (leg1 and leg2). Similarly, the right side of the Figure 8 is the channel current, circulating current and the sum of the channel current of coupled inductor 2 (leg 3 and leg 4) at the same duty cycle.

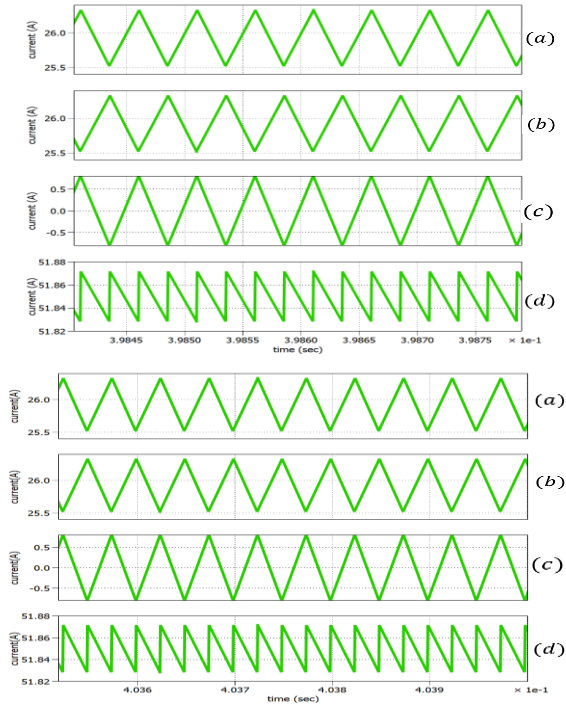


Fig 8: (a) channel 1 (b) channel 2 (c) circulating and (d) output currents; Top: coupled inductor 1 (leg 1&2) (b) Bottom: coupled inductor 2 (Leg 3&4)

From the current waveform shown in Figure 9, a step change is applied in the current reference, and the response of the current controller is observed. It can be observed that prior to the step change, when the converter is operating at a 35% duty cycle, the channel currents are recorded at 17.6 A each, resulting in a total output current of 70 A. Following the current step change, the duty cycle is adjusted to 52%, leading to a near cancellation of the output current. The channel currents are measured to be 26 A each and the channel ripple currents, both before and after the transient, are measured at 0.83 A. The total output current ripple after the step response is measured to be 0.27 A.

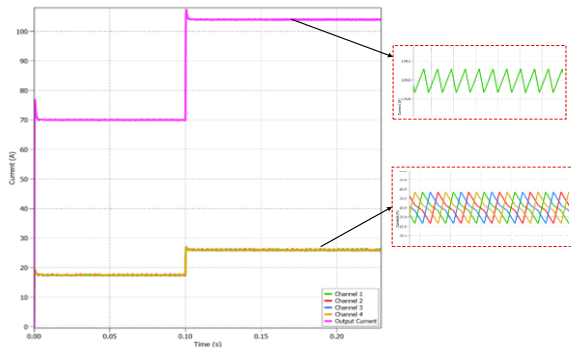


Fig. 9: Steady state performance of the four-channel converter for the channel currents and total output current

waveforms at 35% duty cycle before transient and 52% duty cycle after transient.

The interleaved DC/DC converter is also investigated at multiple operating duty cycles, with the passive components designed for the worst-case operating condition. The converter is capable of operating over the supercapacitor voltage range of 20–250 V, with bidirectional power flow during both charging and discharging. A total current of 104 A is imposed, with an equivalent supercapacitor capacitance of 1.25 F. The reduced equivalent capacitance of 1.25 F, rather than the actual 20.9 F, is used to demonstrate the converter operation over multiple duty cycles within a shorter simulation period. This approach allows all relevant operating points to be captured within a few seconds, rather than requiring a simulation of the entire 35-second operating period, which would be computationally more demanding and make it more difficult to capture the different operating conditions effectively.

From the simulation result, the SC voltage increases its current is positive during charging, while voltage decreases when the current becomes negative implying the SC is discharging. The voltage waveform remains flat when no current flows. The waveforms for the output current, channel currents over the wide operating SC voltage range is shown in Figure 10. Also, the zoomed channel currents and output current are shown to verify the effect of the current ripple cancellation.

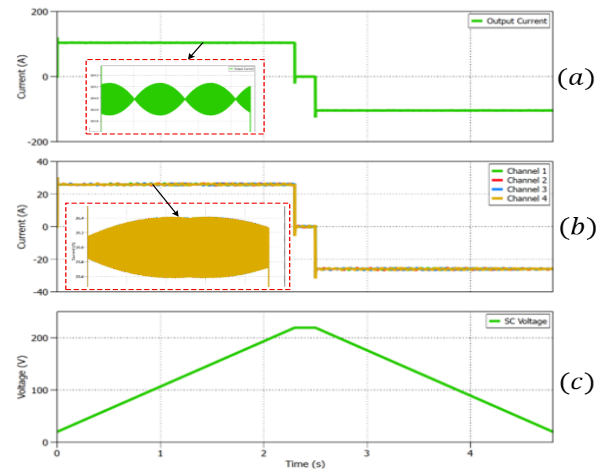


Fig. 10: Wide voltage range operation of the DC/DC converter (a) output current (b) channel currents (c) SC voltage

3.2 Experimental results

The control platform shown in Figure 11 is implemented using the TMS320C6713 DSP/FPGA by Texas Instruments, Dallas, TX, USA, together with a Host Port Interface (HPI) for communication. The DSP operates at a clock frequency of 225 MHz, with sampling and switching frequencies of 20 kHz, and provides a 32-bit external memory interface shared with the FPGA and the daughter card. The daughter card interfaces with the DSP host port to enable code download and bidirectional data exchange with the host computer. The Rohde & Schwarz oscilloscope is used to capture the DC/DC converter waveforms, with a sampling rate of 2.5 GSa/s. The main components used in this experiment are presented in Table 4, together with their summary descriptions. Due to the unavailability of the supercapacitor energy storage system, a DC power supply is used to provide a fixed input voltage of 135 V to the converter, which is half

of the DC-link voltage. This results in an approximately 50% duty cycle and is therefore considered for experimental evaluation. Also in the experiment, two bidirectional power supplies

(SM1500-CP-30) are utilised to serve as the SC pack voltage and DC bus voltage. A scaled-down hardware prototype is developed to validate the bidirectional power flow of the interleaved bidirectional DC/DC converter while maintaining the DC bus voltage and the SC voltage within their specified limits. The setup for the bidirectional DC/DC converter is shown in Figure 12.

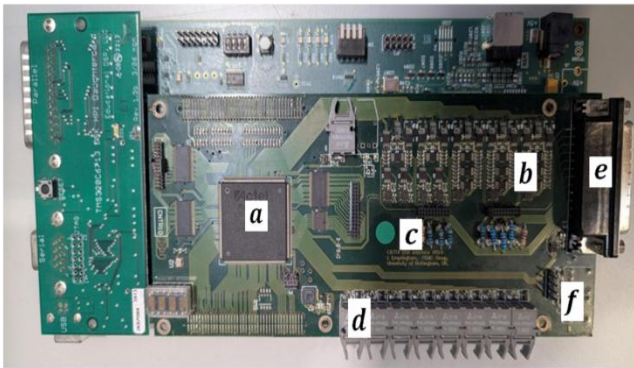


Fig. 11: DSP-FPGA control platform: (a) FPGA chip (b) signal conditioning circuit (c) burden resistors (d) optic fibre transmitters (e) D-type connector (f) reset/enable switch

Table 4: Main components and parameters used in the experiment

Components	Description
DSP/FPGA board	TMS320C6713
SiC Module	CAS100H12AM1 (1.2 kV, 100 A 4xHalf-bridge modules)
Current sensors	LEM LA 55-P
Voltage sensors	LEM LV 25-P
Optic fibre cables	Transmitters and Receivers
Parameters	Values
SC rated voltage: v_{scap}	135 V
DC bus capacitance: C_{bus}	8.0 μ F
DC bus voltage: V_{bus}	270 V
Coupled inductance: L_s, L_m	2.16 mH, 2.12 mH
Common mode inductance: L_k	1.50 mH
Maximum Power	3.40 kW
Switching frequency: f_{sw}	20 kHz

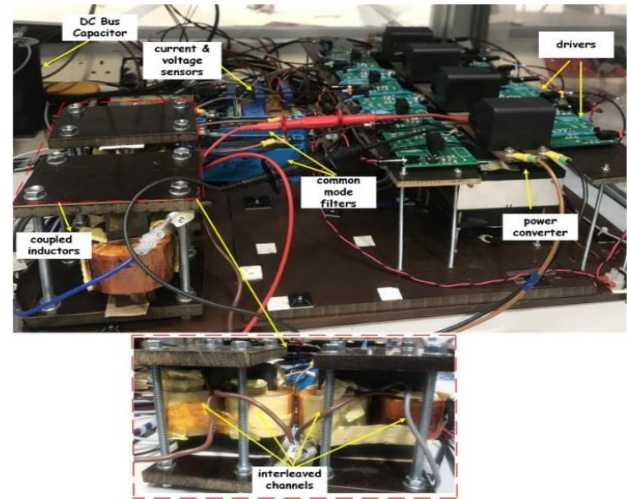


Fig. 12: Experimental setup of the bidirectional DC/DC converter interleaved with coupled inductors

The experimental square waveforms of the gate to source voltage, V_{GS} for the converter measured with four differential voltage probes (by TESTEC and Pico manufacturers) is shown in Figure 12. Channels 1-4 of the half bridge are switched using four PWM signals with each leg phase shifted by $2\pi/2 = 180^\circ$ which are generated using the DSP-FPGA control platform. To avoid shoot-through current between the switching device channels, a small deadtime of 260ns is considered on the each the of device channels.

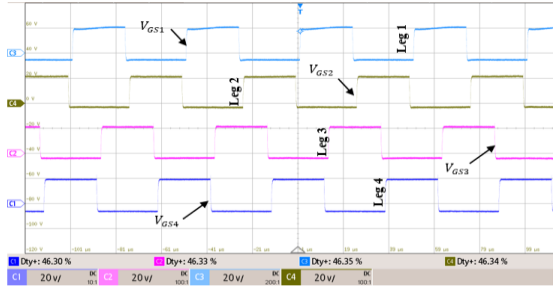


Fig. 12: Gate to source voltages V_{GS} for the four high side switches of each SiC device at 20V/div, 20μs/div

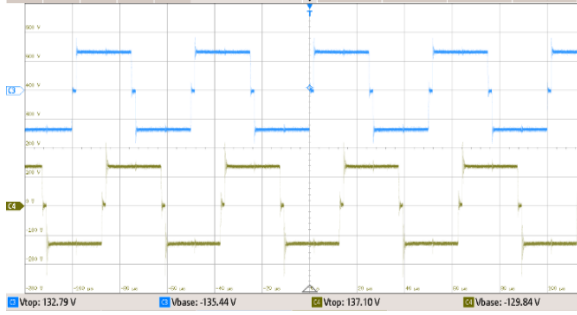


Fig. 13: Line to line voltage waveforms between coupled inductor 1, V_{L12} and coupled inductor 2, V_{L34} phase shifted by 90° at 100V/div, time: 20μs/div

3.3 Transient behaviour of the PI controller

For easy implementation, the converter topology is changed to two channels interleaved and the control behaviour of the converter is first analysed in the experiment before extending to the four-channel

converter. The transient response of the PI controller for the two-channel converter is tuned at varying gains in Figure 14(a) - (f) while the integral time constant is unchanged until the controller instability is reached. From the oscilloscope reading, both the total output, interleaved and circulating currents are in 1A/div at 2msec/div. To get the true dynamics behaviour of the system, a small step current test is chosen to avoid saturating the core. The channel currents i_1 and i_2 were controlled at 3A before the step current and then 4A after the step current. The output current i_{scap} is the sum of the channel current while the circulating current i_c is the difference between the channels. In (a), the current settles fast at 1msec with a 4.5% overshoot a gain k_p of 0.15. In (b) with $k_p=0.20$, it settles at 2msec with 8% overshoot. Increasing k_p to 0.40 in (c), its overshoot current increases to 9% increasing its settling time to 3msec. At this point, the controller stability reduces as well as (d). In (e), the settling time is reduced to 6msec with 14% overshoot. At $k_p=0.80$ in (f), the response of the controller becomes marginally unstable. From the observation, it can be seen the gain at $k_p=0.15$ has the best controller response with fast settling time of 1ms with minimum current overshoot of 4.5% which closely matches with the simulation results in the previous chapter.

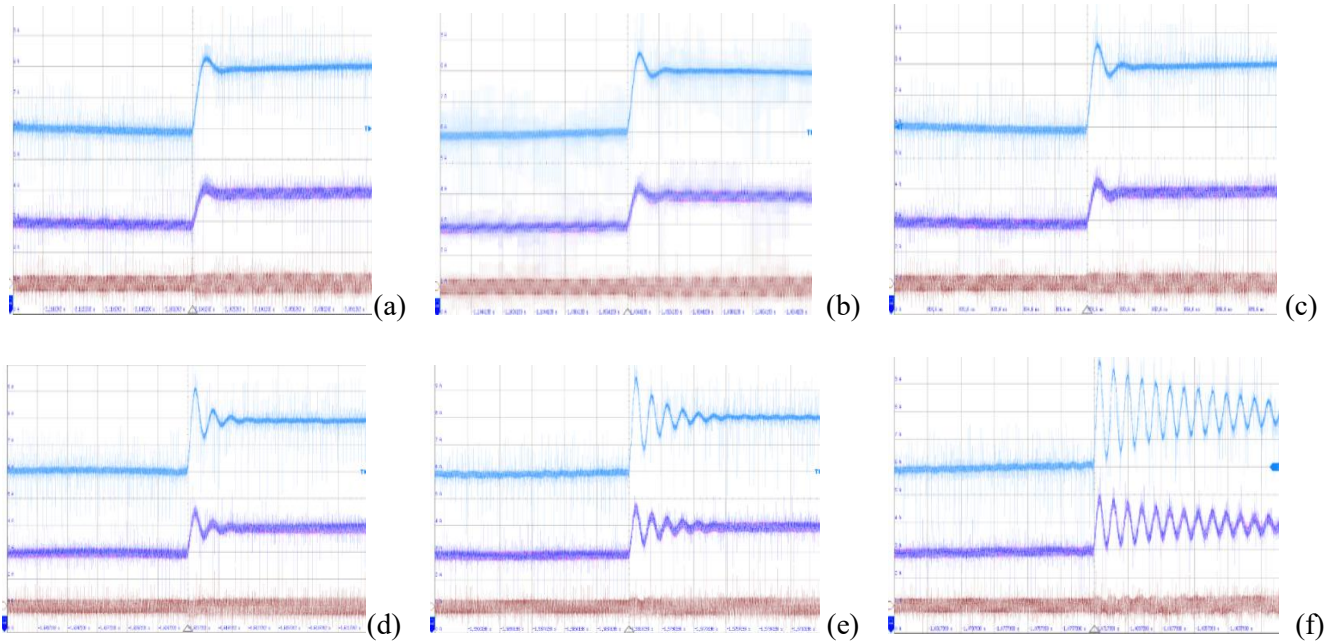


Fig. 14: Transient response measured at varying gains with oscilloscope reading 1A/div, 2ms/div: (a) $k_p=0.15$ (b) $k_p=0.20$ (c) $k_p=0.25$ (d) $k_p=0.40$ (e) $k_p=0.60$ (f) $k_p=0.80$ oscillatory

Figure 15 presents the transient and steady-state response of the bidirectional converter under charging and discharging conditions. During discharging operation, high power is drawn from the SC side to the aircraft DC bus, resulting in a negative current, where the measured total current, i_{scap} is -25.5 A. One channel of the interleaved current, i_1 , is also captured and measured to be approximately -6.3 A. A step response is applied when the bidirectional converter transitions to charging mode, during which current charges the SC energy storage system. Under this condition, the total current and channel 1 current are measured to be 25.5 A and 6.3 A, respectively. Throughout all operating conditions, the DC bus voltage, V_{bus} remains constant at 270 V, as shown in the figure.

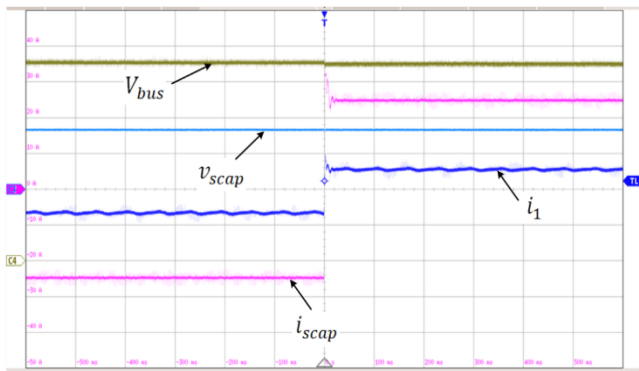


Fig. 15: Experimental results for bidirectional load demand during charging and discharging conditions: i_{scap} , i_1 (10A/div) and V_{bus} , v_{scap} (50V/div) at 100ms/div

4. CONCLUSION

This paper presents the optimal design of a supercapacitor energy storage system to achieve minimum weight, together with the simulation of a bidirectional DC/DC converter employing coupled inductors. For easy implementation, the experimental work starts with a closed loop of two channels interleaved (one coupled inductor) DC/DC converter before extending to four channels (2 coupled inductor) interleaved DC/DC converter. The proposed application is intended to satisfy the peak power demand of an aircraft during the take-off phase. The converter control system is implemented to ensure equal current sharing among the interleaved phases through a phase-balancing strategy, while also enabling bidirectional power flow between the energy storage

system and the aircraft DC bus. Reduced-scale experimental results are also presented to validate the simulation results.

REFERENCES

- [1] A. Barzkar and M. Ghassemi, "Electric power systems in more and all electric aircraft: A review," *IEEE Access*, vol. 8, pp. 169314–169332, 2020, doi: 10.1109/ACCESS.2020.3024168.
- [2] L. Tong, Q. Wei, X. Wen, K. Wang, and J. Ding, "The Impact of Digitalized All-Electric Aircraft on the Sustainable Development of the Aviation Industry: A Dynamic Differential Game Study Considering Delayed Effects," *Sustain.*, vol. 17, no. 22, pp. 1–34, 2025, doi: 10.3390/su172210288.
- [3] A. Fares, C. Klumpner, and M. Rashed, "Design Considerations to Optimise Supercapacitor-based Energy Storage Systems for Aerospace Applications," *2018 IEEE Int. Conf. Electr. Syst. Aircraft, Railw. Sh. Propuls. Road Veh. Int. Transp. Electrification Conf. ESARS-ITEC 2018*, 2019, doi: 10.1109/ESARS-ITEC.2018.8607796.
- [4] M. Al Takroui *et al.*, "A Comparison Study of Hybrid Energy Storage System Topologies for Electric Vehicles," *IEEE Access*, vol. 12, no. September, pp. 171675–171688, 2024, doi: 10.1109/ACCESS.2024.3476513.
- [5] A. Abubakar, C. Klumpner, and P. Wheeler, "A Multiport / Multiphase DC / DC Converter with Coupled Inductors for Hybrid Energy Storage Systems Suitable for Aircraft Applications," *machines* MDPI, pp. 1–23, 2026 doi.org/10.3390/machines14050490
- [6] S. D. Sandeep, S. Mohanty, S. B. Mohanty, and P. S. Puan, "A comprehensive review on DC microgrid control and energy management strategies," *Results Eng.*, vol. 26, no. January, p. 105479, 2025, doi: 10.1016/j.rineng.2025.105479.
- [7] R. Mohan, Undeland, *Power Electronics: Converters, Applications, and Design*. John Wiley & Sons; 2nd Edition (23 Mar. 1995).

- [8] G. Guidi, T. M. Undeland, and Y. Hori, "An interface converter with reduced volt-ampere ratings for battery-Supercapacitor mixed systems," *IEEE Trans. Ind. Appl.*, vol. 128, no. 4, pp. 2–7, 2008, doi: 10.1541/ieejias.128.418.
- [9] M. A. Chewale, R. A. Wanjari, V. B. Savakhande, and P. R. Sonawane, "A Review on Isolated and Non-isolated DC-DC Converter for PV Application," *2018 Int. Conf. Control. Power, Commun. Comput. Technol. ICCPCCT 2018*, pp. 399–404, 2018, doi: 10.1109/ICCPCCT.2018.8574312.
- [10] R. Swarnkar, H. K. Verma, and R. N. Patel, "Comparative Analysis of Isolated and Non-Isolated Bi-Directional DC-DC Converters for DC Microgrid," *2019 3rd Int. Conf. Recent Dev. Control. Autom. Power Eng. RDCAPE 2019*, pp. 557–562, 2019, doi: 10.1109/RDCAPE47089.2019.8979027.
- [11] R. Rajesh, N. Prabakaran, and T. K. Santhosh, "Design and Analysis of a Non-Isolated DC-DC Converter With a High-Voltage Conversion Ratio," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 70, no. 6, pp. 2036–2041, 2023, doi: 10.1109/TCSII.2022.3226187.
- [12] Z. Wang, P. Wang, H. Bi, and M. Qiu, "A bidirectional DC/DC converter with wide-voltage gain range and low-voltage stress for hybrid-energy storage systems in electric vehicles," *J. Power Electron.*, vol. 20, no. 1, pp. 76–86, 2020, doi: 10.1007/s43236-019-00017-2.
- [13] H. Wu, J. Lu, W. Shi, and Y. Xing, "Nonisolated bidirectional dc-dc converters with negative-coupled inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2231–2235, 2012, doi: 10.1109/TPEL.2011.2180540.
- [14] L. Schmitz, D. C. Martins, and R. F. Coelho, "Comprehensive conception of high step-Up DC-DC converters with coupled inductor and voltage multipliers techniques," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 67, no. 6, pp. 2140–2151, 2020, doi: 10.1109/TCSI.2020.2973154.
- [15] M. Gerber, J. A. Ferreira, I. W. Hofsjager, and N. Seliger, "Interleaving optimization in synchronous rectified DC/DC converters," *PESC Rec. - IEEE Annu. Power Electron. Spec. Conf.*, vol. 6, pp. 4655–4661, 2004, doi: 10.1109/PESC.2004.1354823.
- [16] H. Cheaito, B. Allard, and G. Clerc, "Proof of concept of 35 kW electrical taxiing system in more electrical aircraft for energy saving," *Int. J. Electr. Power Energy Syst.*, vol. 130, no. January, 2021, doi: 10.1016/j.ijepes.2021.106882.
- [17] D. Baba, "Benefits of a multiphase buck converter," *Texas Instruments*, no. 1, pp. 8–13, 2012.
- [18] R. R. de Melo, F. L. Tofoli, S. Daher, and F. L. M. Antunes, "Interleaved bidirectional DC–DC converter for electric vehicle applications based on multiple energy storage devices," *Electr. Eng.*, vol. 102, no. 4, pp. 2011–2023, 2020, doi: 10.1007/s00202-020-01009-3.
- [19] M. S. A. Jafarian and H. R. Karshenas, "Current ripple reduction in single-input, multiple-output converters using phase-shift and coupled inductors," *2016 24th Iran. Conf. Electr. Eng. ICEE 2016*, pp. 816–821, 2016, doi: 10.1109/IranianCEE.2016.7585632.
- [20] C. Chang and M. A. Knights, "Interleaving Technique in Distributed Power Conversion Systems," vol. 42, no. 5, 1995.
- [21] P. Magne, P. Liu, B. Bilgin, and A. Emadi, "Investigation of impact of number of phases in interleaved de-de boost converter," *2015 IEEE Transp. Electrification Conf. Expo, ITEC 2015*, 2015, doi: 10.1109/ITEC.2015.7165754.
- [22] R. Mayer, M. B. El Kattel, and S. V. G. Oliveira, "Multiphase Interleaved Bidirectional DC/DC Converter with Coupled Inductor for Electrified-Vehicle Applications," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2533–2547, 2021, doi: 10.1109/TPEL.2020.3015390.
- [23] M. Hagemeyer, F. Schafmeister, and J. Bocker, "Coupled Inductor Design for Interleaved High-

- Current DC-DC Converters,” *ICEMS 2018 - 2018 21st Int. Conf. Electr. Mach. Syst.*, pp. 2316–2321, 2018, doi: 10.23919/ICEMS.2018.8549503.
- [24] A. Abubakar, C. Klumpner, and P. Wheeler, “Optimal Design of Energy Storage System for Electric Aircraft,” *2025 Energy Convers. Congr. Expo Eur. ECCE Eur. 2025 - Proc.*, pp. 1–6, 2025, doi: 10.1109/ECCE-Europe62795.2025.11238947.
- [25] P. Saenger, N. Devillers, K. Deschinkel, M. C. Pera, R. Couturier, and F. Gustin, “Optimization of Electrical Energy Storage System Sizing for an Accurate Energy Management in an Aircraft,” *IEEE Trans. Veh. Technol.*, vol. 66, no. 7, pp. 5572–5583, 2017, doi: 10.1109/TVT.2016.2617288.
- [26] M. Uno and A. Kukita, “Cycle Life Evaluation Based on Accelerated Aging Testing for Lithium-Ion Capacitors as Alternative to Rechargeable Batteries,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1607–1617, 2016, doi: 10.1109/TIE.2015.2504578.
- [27] D. B. Murray and J. G. Hayes, “Cycle testing of supercapacitors for long-life robust applications,” *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2505–2516, 2015, doi: 10.1109/TPEL.2014.2373368.
- [28] P. Backup, “Designing with Supercapacitors Abracon Power Backup,” 2024. www.abracon.com (accessed May 06, 2026).
- [29] A. M. Fares, M. Kippke, M. Rashed, and C. Klumpner, “Development of a Smart Supercapacitor Energy Storage System for Aircraft Electric Power Systems,” *2021 Energies* 2021, 14, 8056. <https://doi.org/10.3390/en14238056>
- [30] A. M. Fares, C. Klumpner, and M. Sumner, “A Novel Multiport DC-DC Converter for Enhancing the Design and Performance of Battery–Supercapacitor Hybrid Energy Storage Systems for Unmanned Aerial Vehicles,” *Appl. Sci.*, vol. 12, no. 6, 2022, doi: 10.3390/app12062767.
- [31] T. Electronics, “Ferrites and accessories Core set,” 2013. <https://www.tdk-electronics.tdk.com/download/528850/d7dcd087c9a2dbd3a81365841d4aa9a5/pdf-n27.pdf>.
- [32] T. Electronics, “Ferrites and Accessories Core,” 2013. <https://www.tdk-electronics.tdk.com/download/540184/3a7f957d754f899aec42cd946598c5c4/pdf-n27.pdf>.